

EAST - [10043000.wsp:1]

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Default operator: OR

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((diagonal adj interconnection) and (substrate or board)) and plurality) not (((diagonal adj interconnection) and (substrate or board)) and plurality) and (integrated adj circuit))

US 6504841 20030107 50 Three-dimensional interconnection geometr. 370/386 340/825.5 Larson, Brian B1

US 6298438 20011002 33 System and method for 712/226 712/223; Thayer, John S. et al. B1

US 6215786 20010410 40 Implementation of 370/386 340/825.5 Larson, Brian B1

US 6215504 20010410 33 Line drawing using 345/443 Ralph et al. B1

US 6173366 20010109 34 Load and store 711/129 710/66; Thayer, John S. et al. B1

US 6154831 20001128 34 Decoding operands for 712/208 712/22; Thayer, John S. et al. A

US 6141673 20001031 32 Microprocessor modified 708/402 708/401; Thayer, John S. et al. A

US 6061521 20000509 31 Computer having 712/9 708/520; Thayer, John S. et al. A

US 6047372 20000404 33 Apparatus for routing 712/222 712/5; Thayer, John S. et al. A

US 6009505 19991228 32 one operand to an arith. 712/7 Thayer, John S. et al. A

US 6006245 19991221 31 System and method for 712/6 708/514; Thayer, John S. et al. A

US 5991865 19991123 23 routing one operand to 708/520; Thayer, John S. et al. A

Enhanced fast fourier transform technique on MPEG motion compensation using oper. 712/7 712/14; Longhenry, Brian E. et al.

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